CLAIM AMENDMENTS:

Claims 1-23 (Canceled)

24 (Original) A method of forming a trench DMOS transistor device comprising:

providing a substrate of a first conductivity type, said substrate acting as a common drain region for said device;

depositing an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

forming an insulating layer lining at least a portion of said trench;

forming a conductive region within said trench adjacent said insulating layer;

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench; and

forming a low resistivity deep region extending into said device from an upper surface of said epitaxial layer, said deep region acting to provide electrical contact with said substrate.

25 (Original) The method of claim 24, wherein said deep region comprises a semiconductor region of said first conductivity type that is formed by an implantation and diffusion process.

26 (Original) The method of claim 24, wherein said deep region comprises a metallic region, and wherein said deep region is formed by a process comprising etching a deep trench that extends into said device from an upper surface of said epitaxial layer, and depositing metal within said deep trench.

27 (Original) The method of claim 24, wherein said deep region comprises a doped polysilicon region, and wherein said deep region is formed by a process comprising etching a deep trench

that extends into said device from an upper surface of said epitaxial layer, and depositing polysilicon within said deep trench.

28 (Original) The method of claim 24, further comprising: forming a metallic drain contact adjacent an upper surface of said deep region, forming a metallic source contact adjacent an upper surface of said source region, and forming a metallic gate contact adjacent an upper surface of said conductive region in a termination region remote from said source region.

29 (Original) The method of claim 24, wherein said low resistivity deep region has a resistivity of 0.01 Ohm-cm or less and extends at least 20 % of the distance from said upper surface of said epitaxial layer to said substrate.

30 (Original) The method of claim 29, wherein said low resistivity deep region extends from said upper surface of said epitaxial layer to said substrate.